



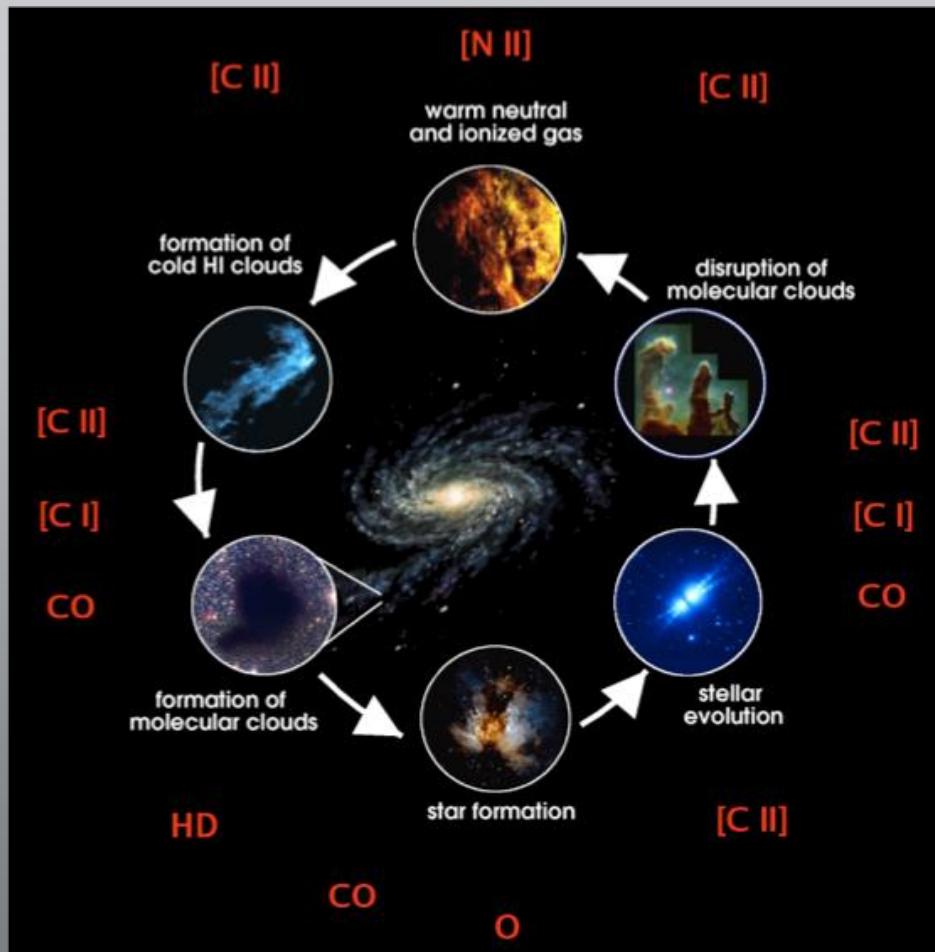
# 4-Pixel Heterodyne Receiver at 1.9 THz using a CMOS Spectrometer

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Pasadena, CA 91109, USA*

<sup>2</sup>*Observatoire de Paris, 75014 Paris, France*

# Lifecycle of the ISM



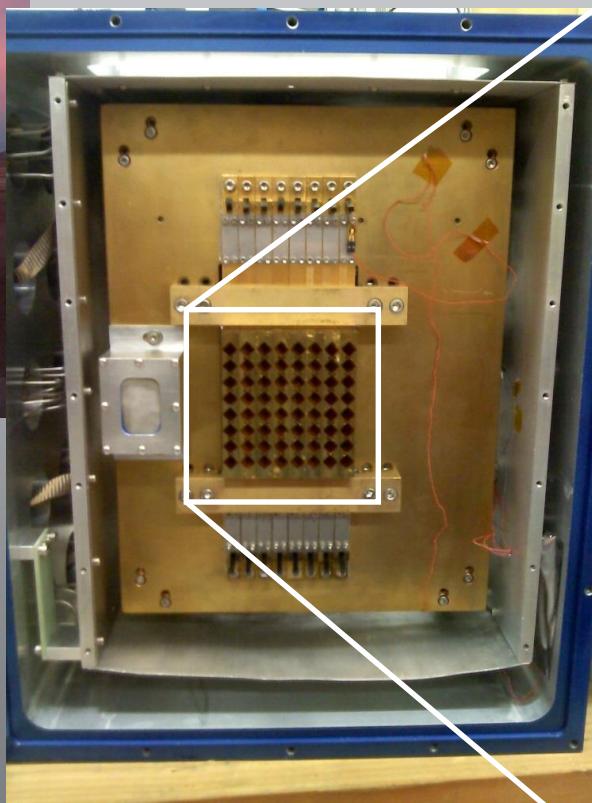
Large spectroscopic THz arrays are needed for surveys that can disentangle the motions of giant molecular clouds (GMCs) in the ISM.



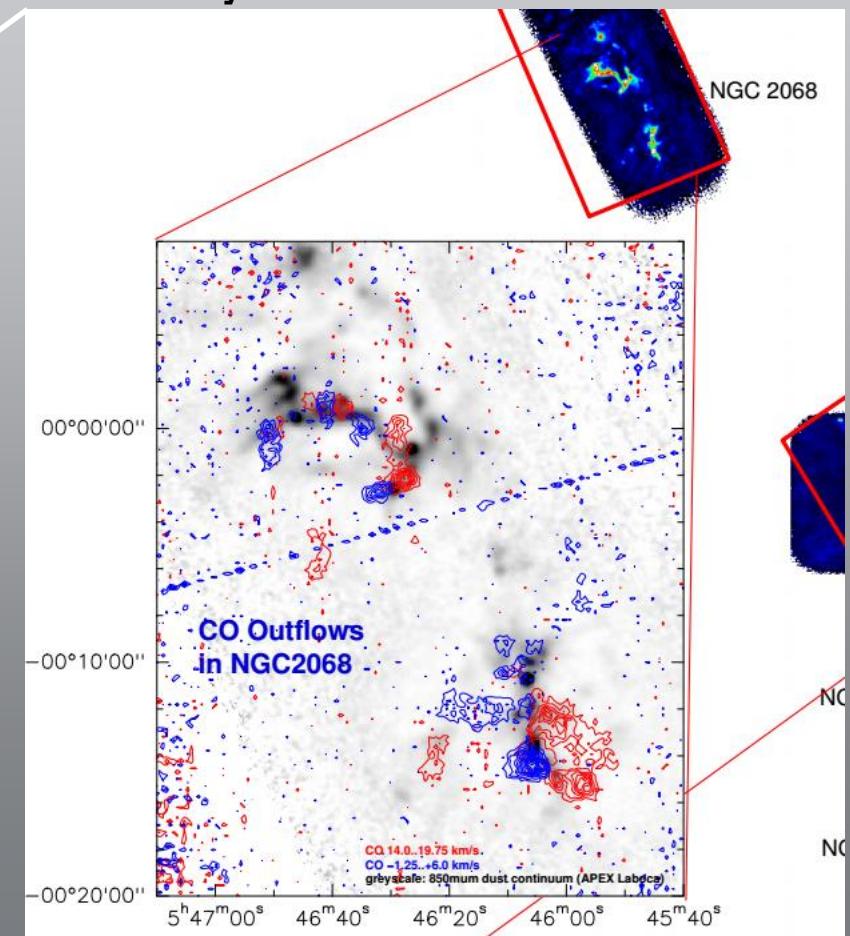
# CO Survey Instrument: SuperCam



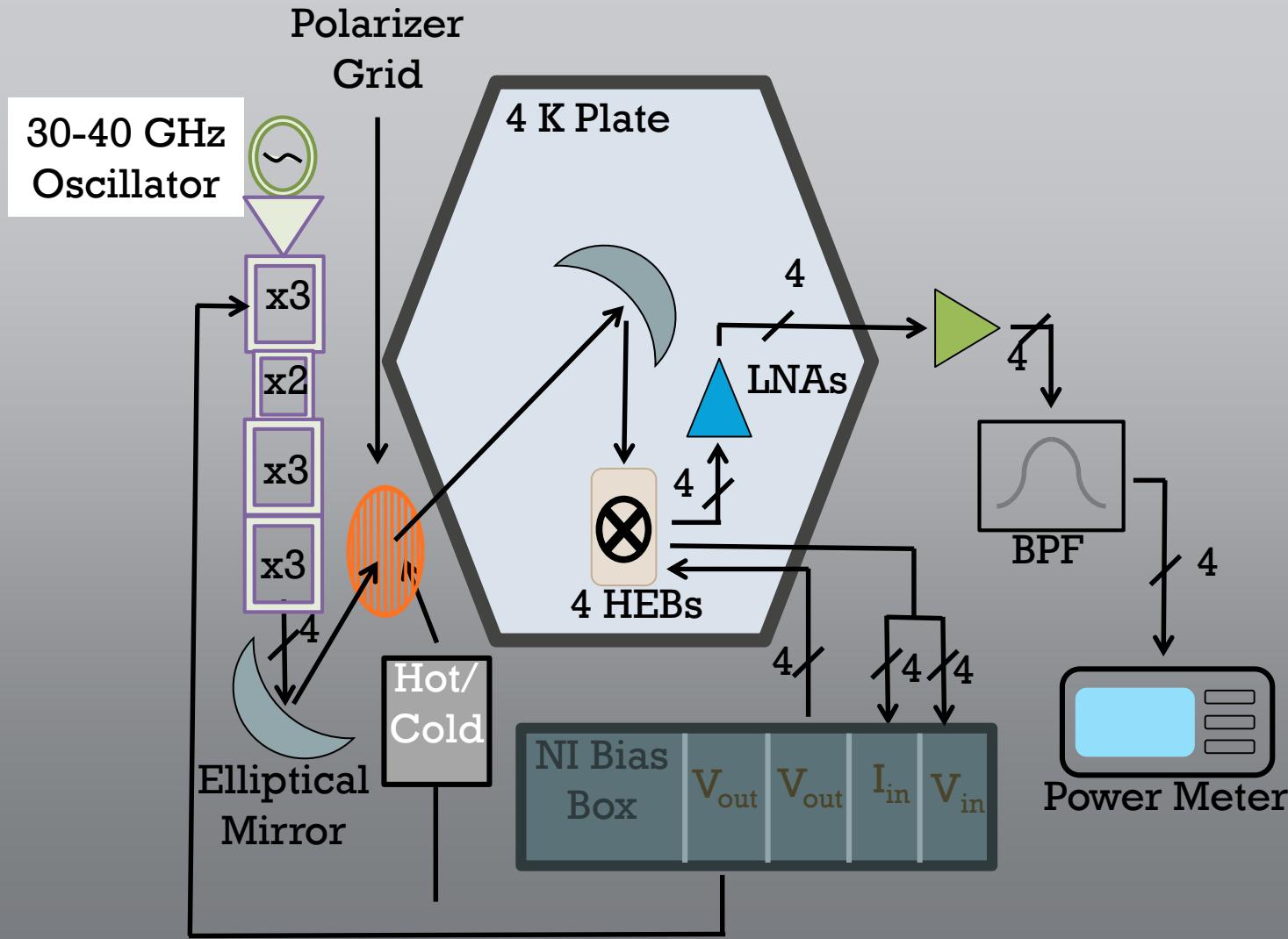
APEX



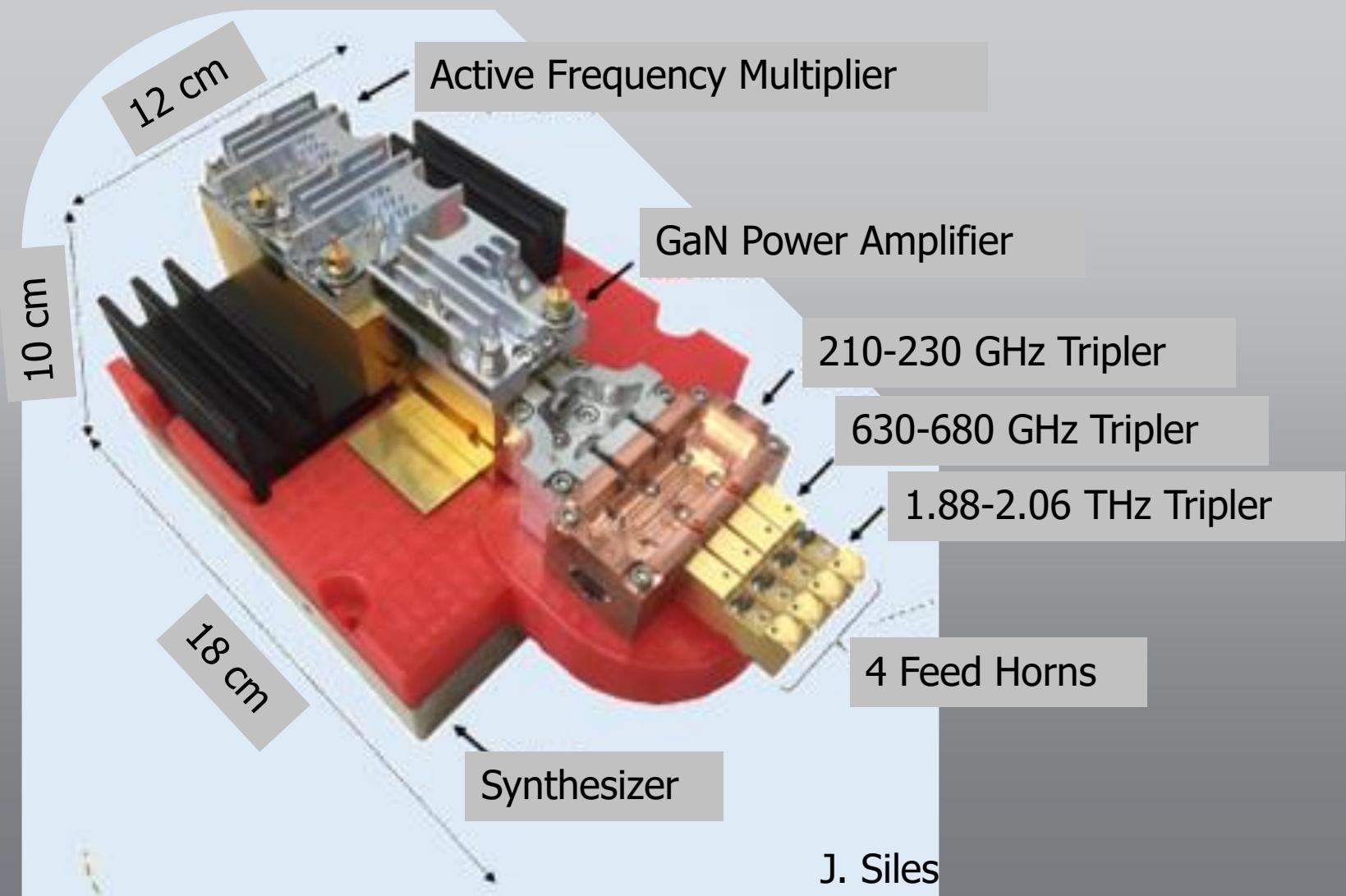
Courtesy of T. Stanke



# Lab Setup

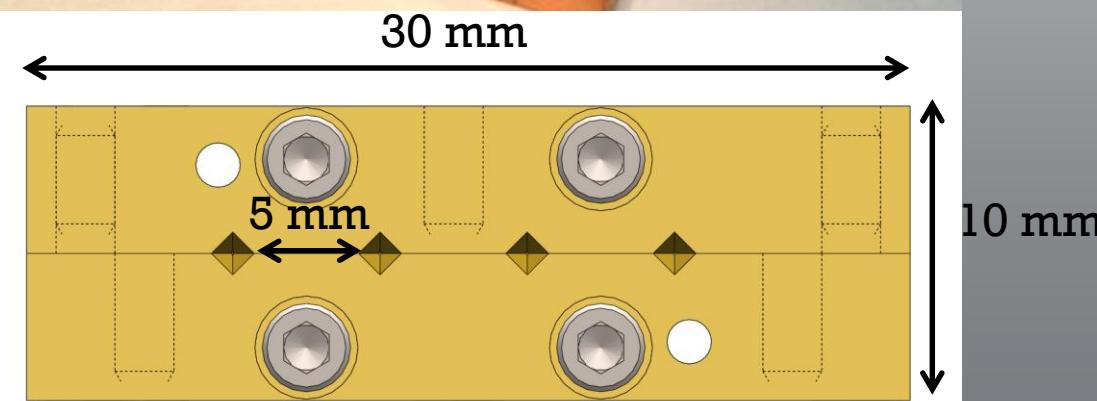
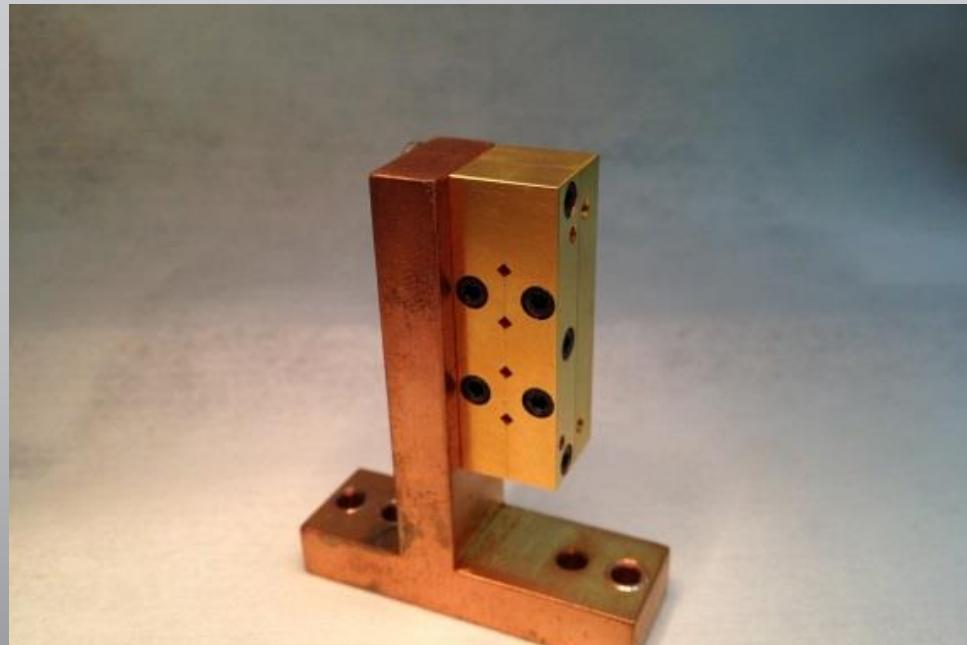


# Local Oscillator: 4-Pixel Multiplier Chain





# 4-Pixel Mixer Block





# Mixers

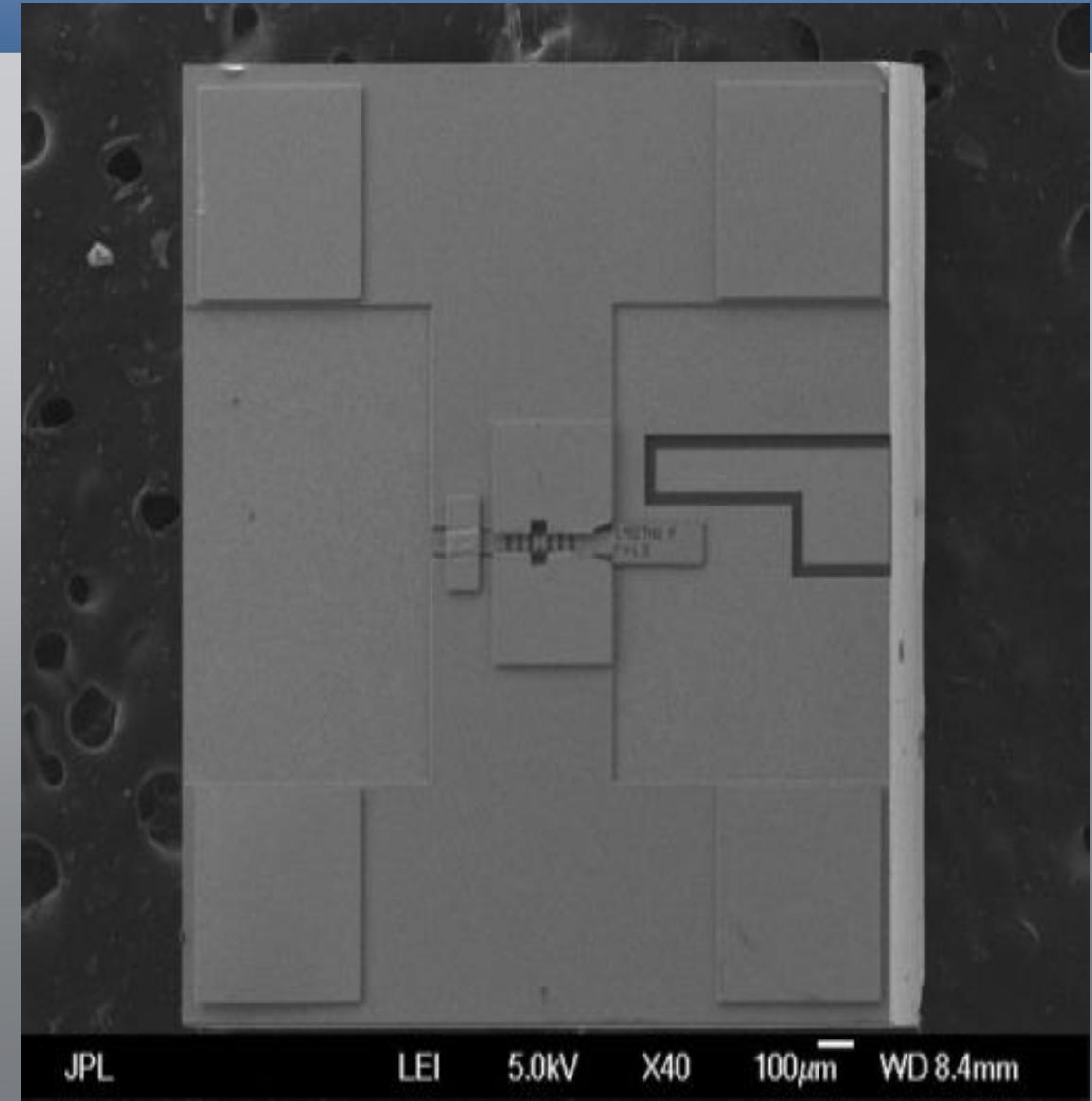
SOI Chip-  
HEB  
Technology





# Mixers

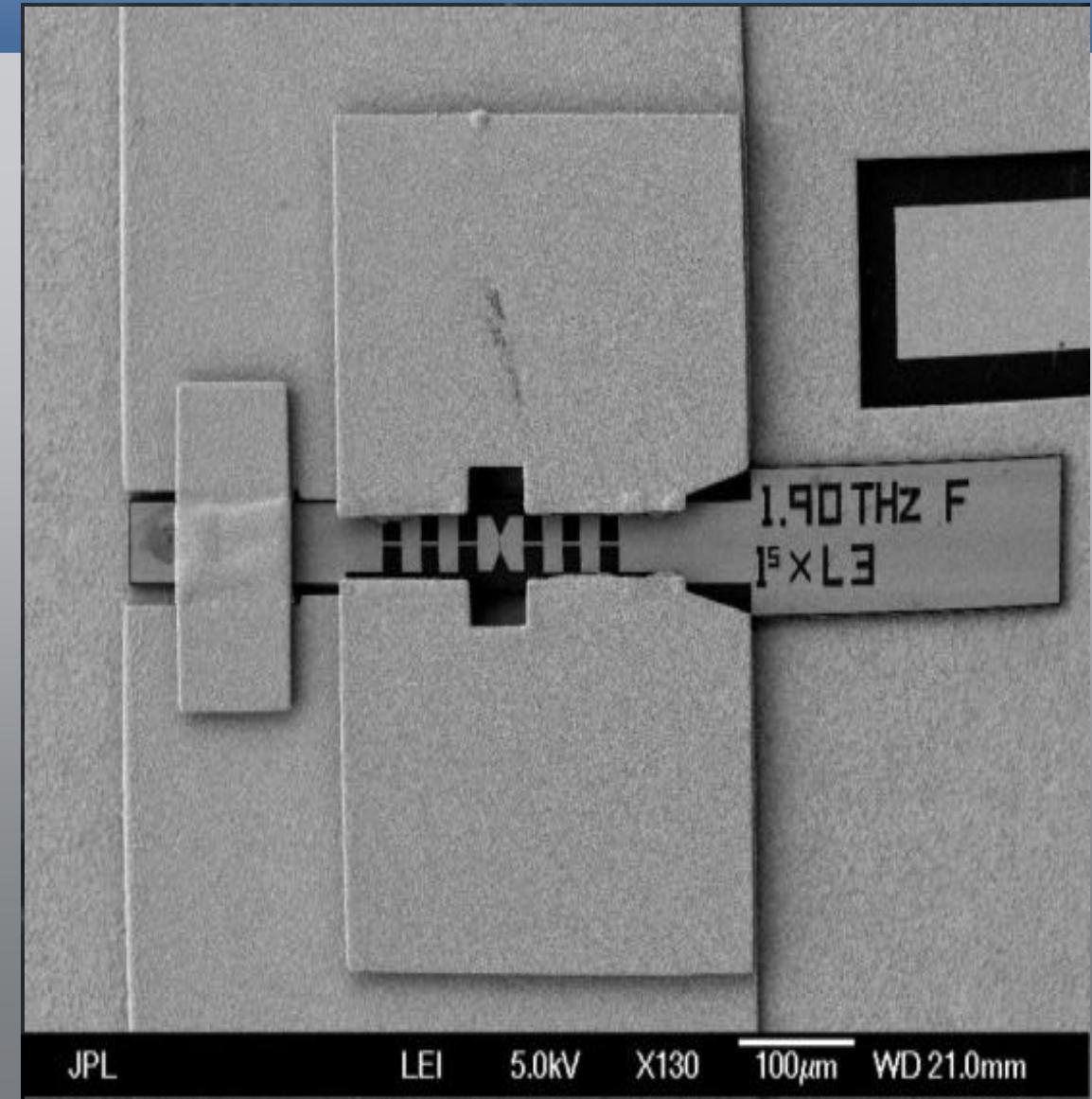
SOI Chip-  
HEB  
Technology

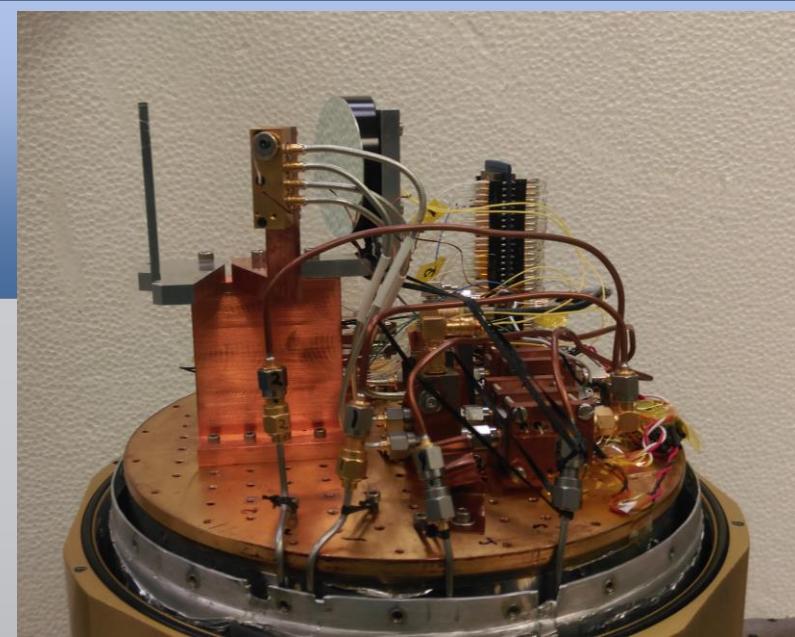
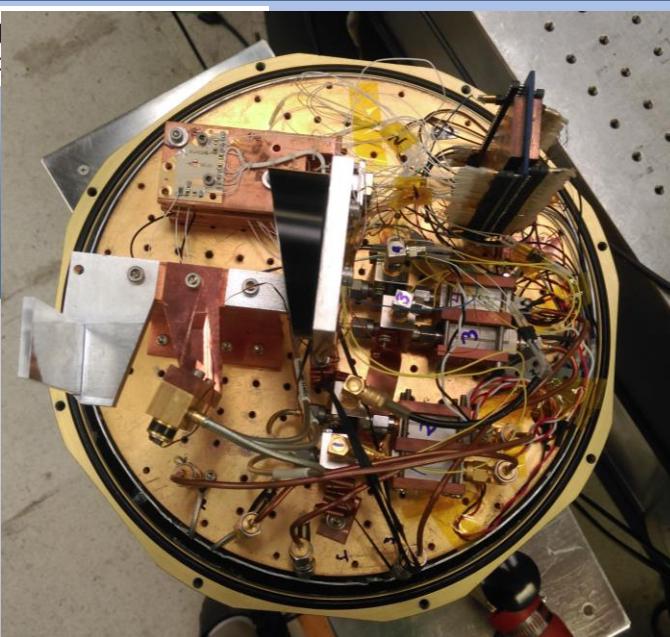




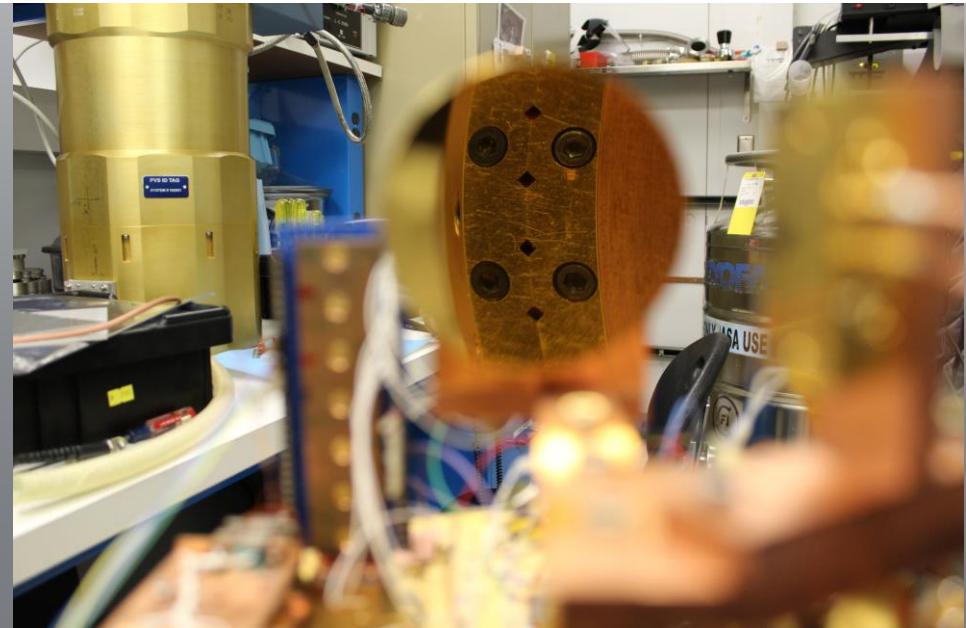
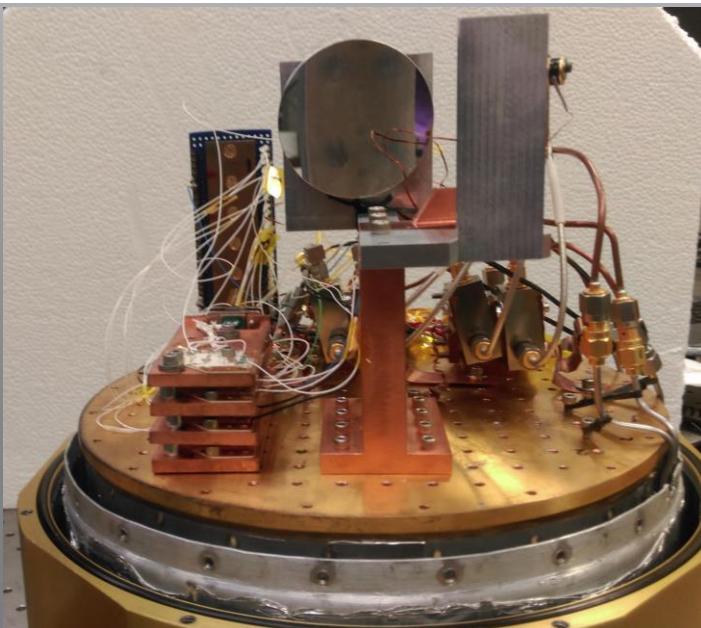
# Mixers

SOI Chip-  
HEB  
Technology



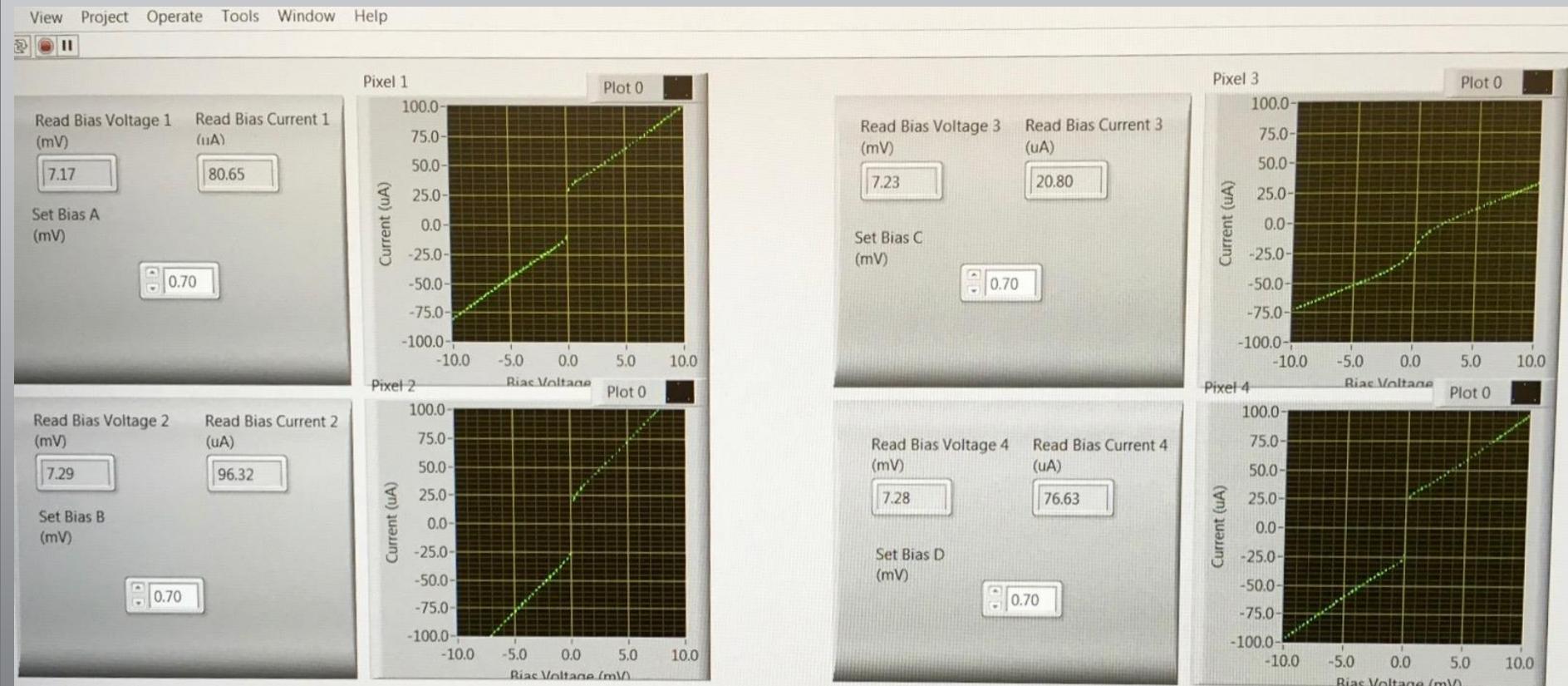


# 4 Pixel Array Inside the Cryostat



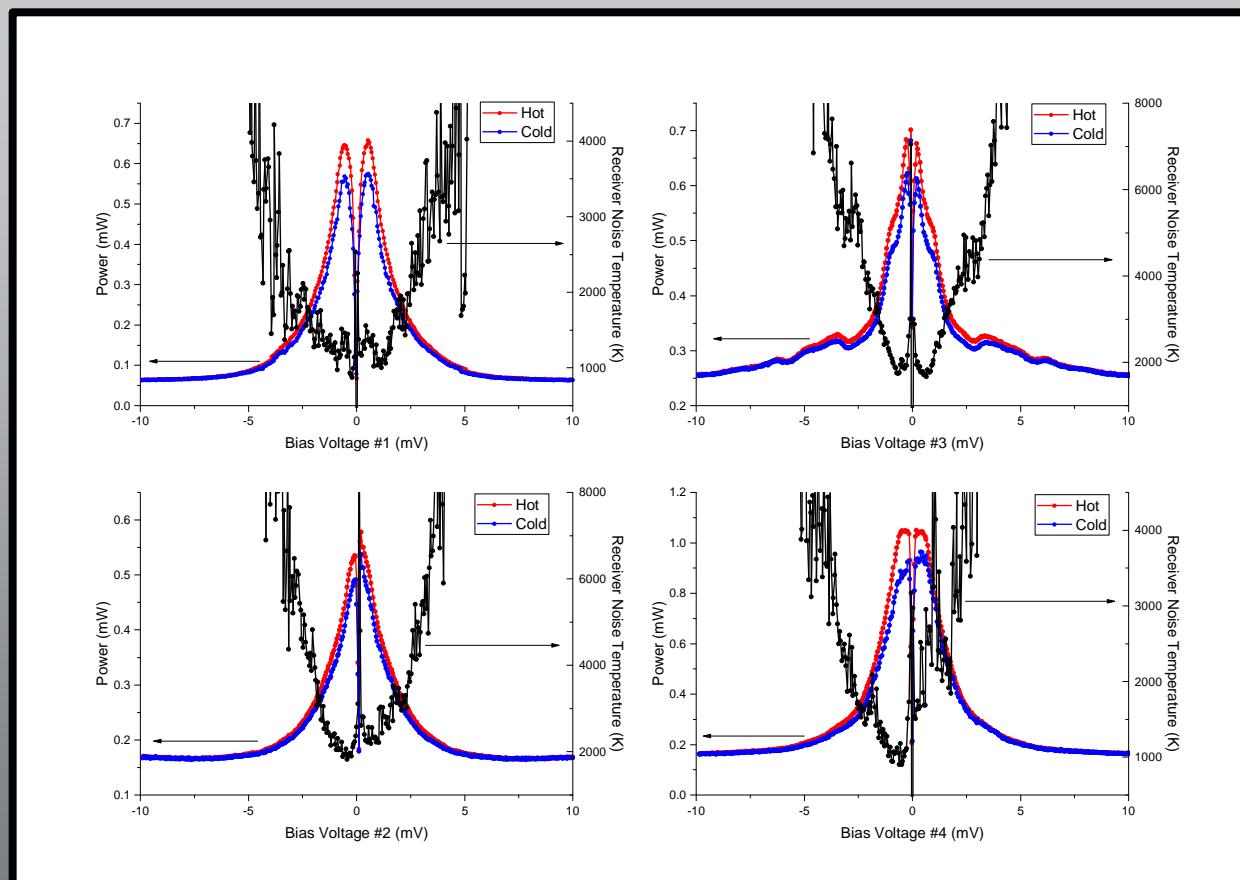


# Lab Results



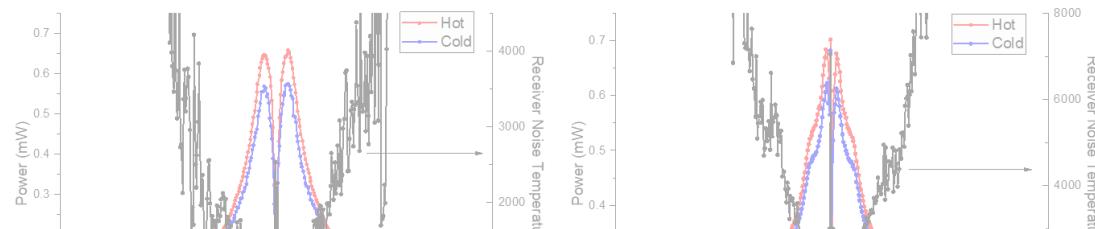
# Lab Results

Using an IBOB spectrometer



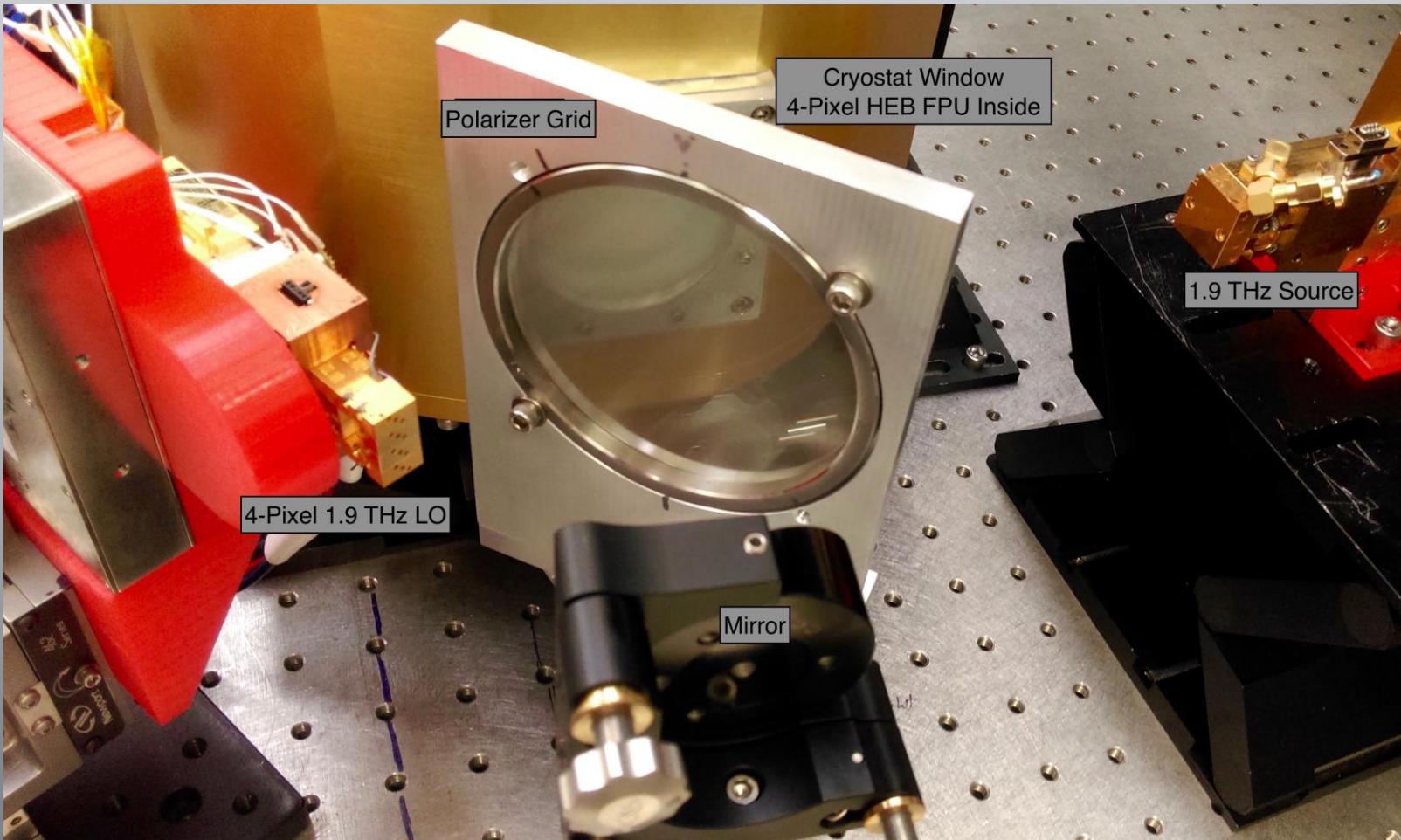
# Lab Results

Using an IBOB spectrometer



Pixel	$\Omega_{\text{RT}}$ ( $\Omega$ )	$\Omega_{100\text{K}}$ ( $\Omega$ )	$I_c$ ( $\mu\text{A}$ )	$T_{\text{RX, DSB}}$ (K)
1	109	126	130	900
2	82	93	165	1800
3	130	179	30	1700
4	105	120	185	900

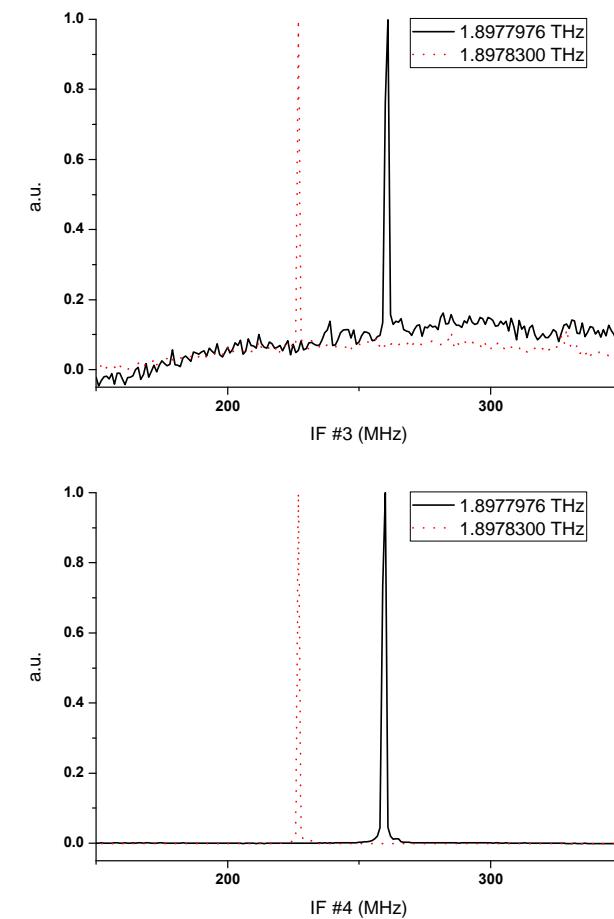
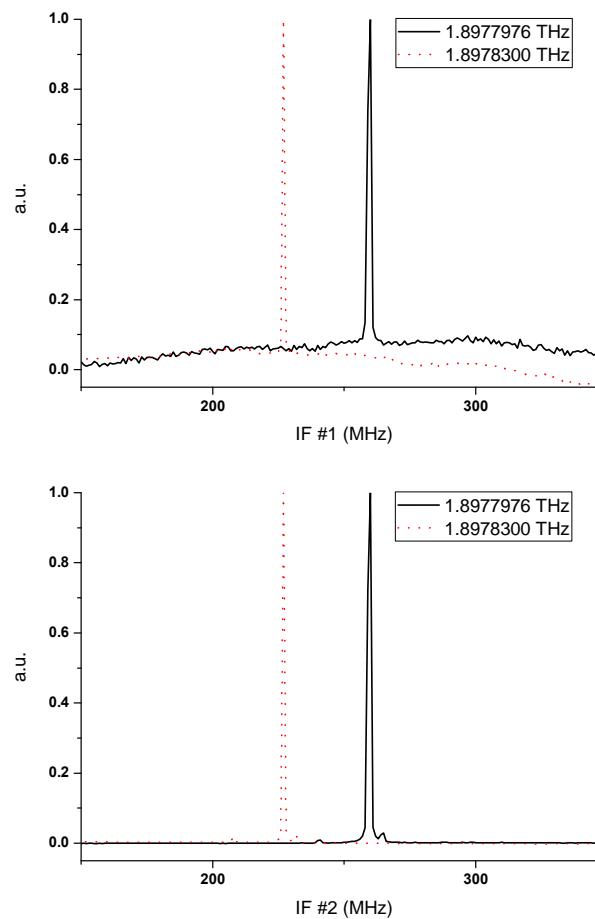
# Lab Setup for 1.9 THz Spectra



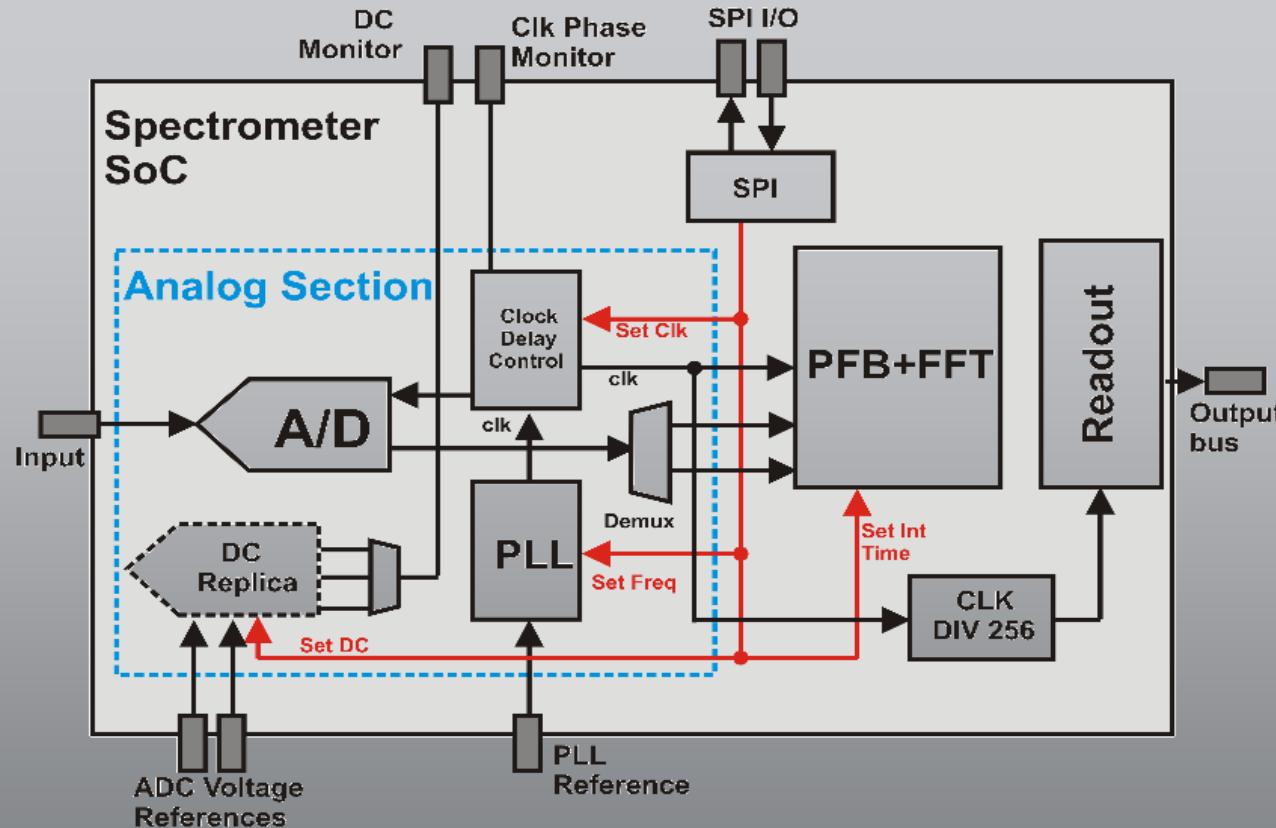
Measurement setup for 4-pixel heterodyne array receiver verification at 1.9 THz.

# Lab Results

Using an IBOB  
spectrometer



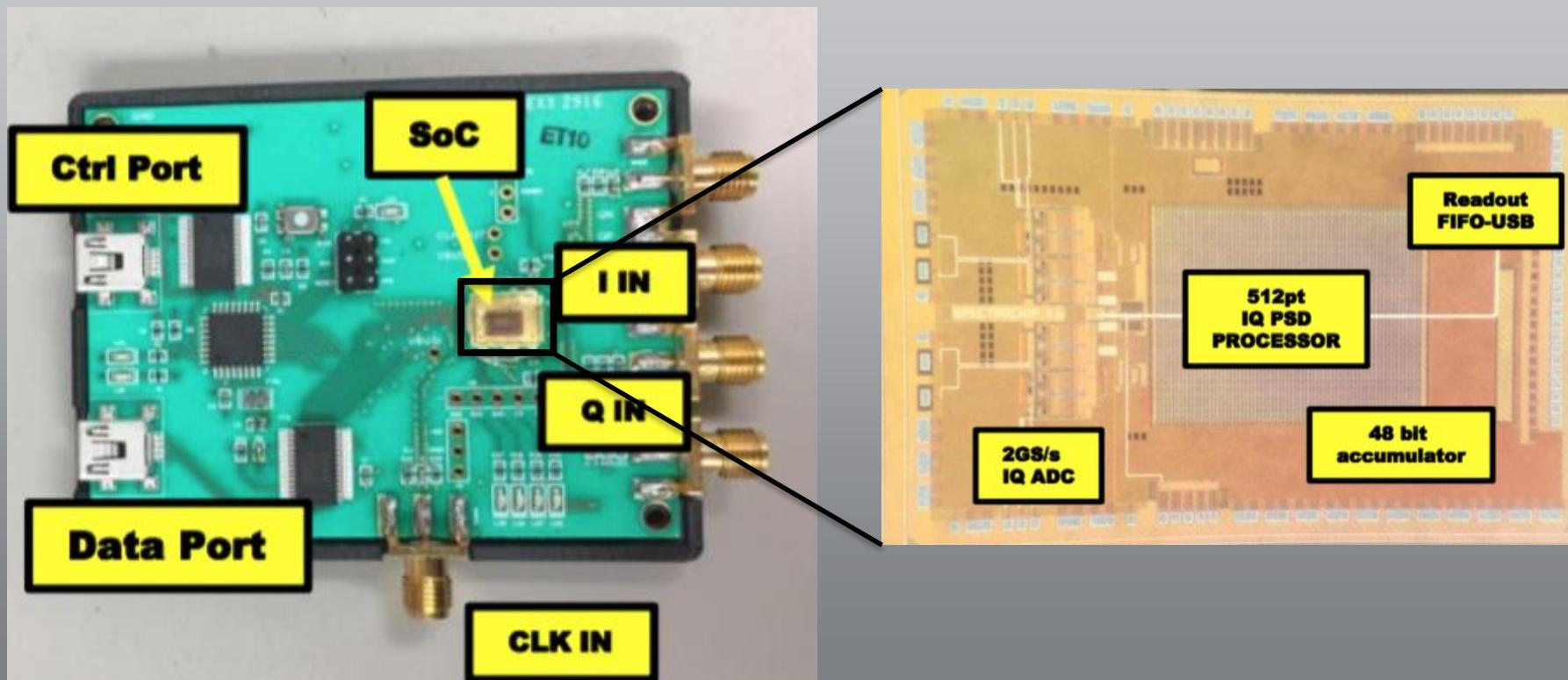
# CMOS Spectrometer Processor Development



Joint UCLA-JPL developed system-on-chip (SoC) contain digitizers, FFT processors, and USB readout circuitry to provide highly integrated and low-power spectral processing.

# CMOS Spectrometer Processor Development

## 2.0 GS/s Complex FFT Version





# CMOS Spectrometer

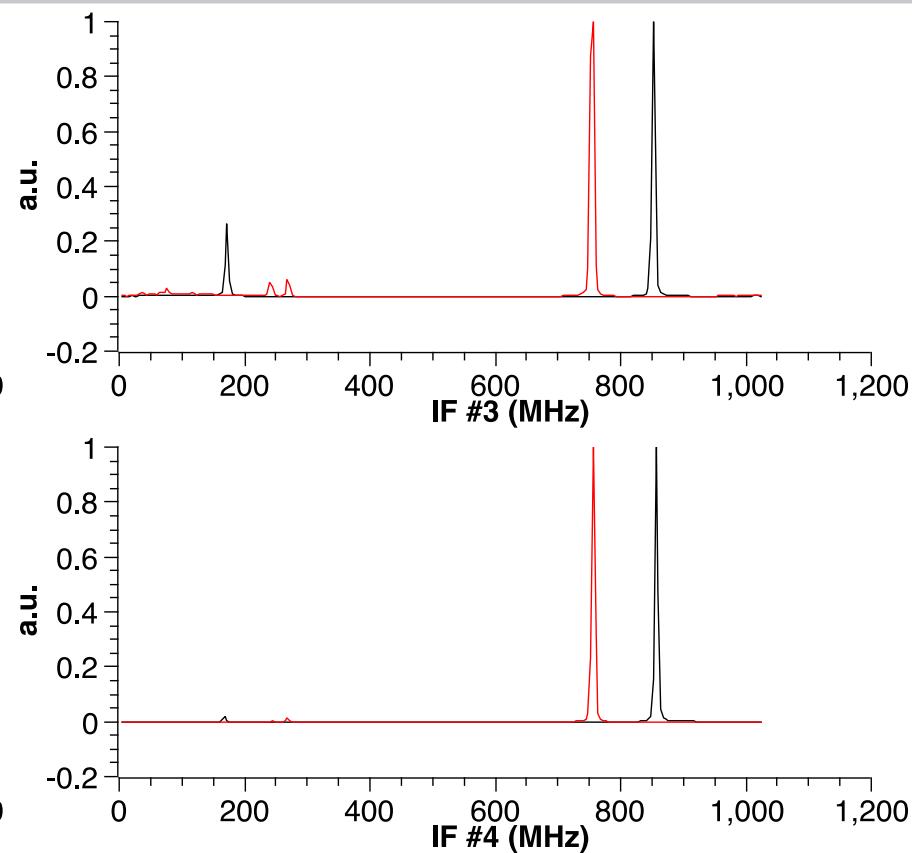
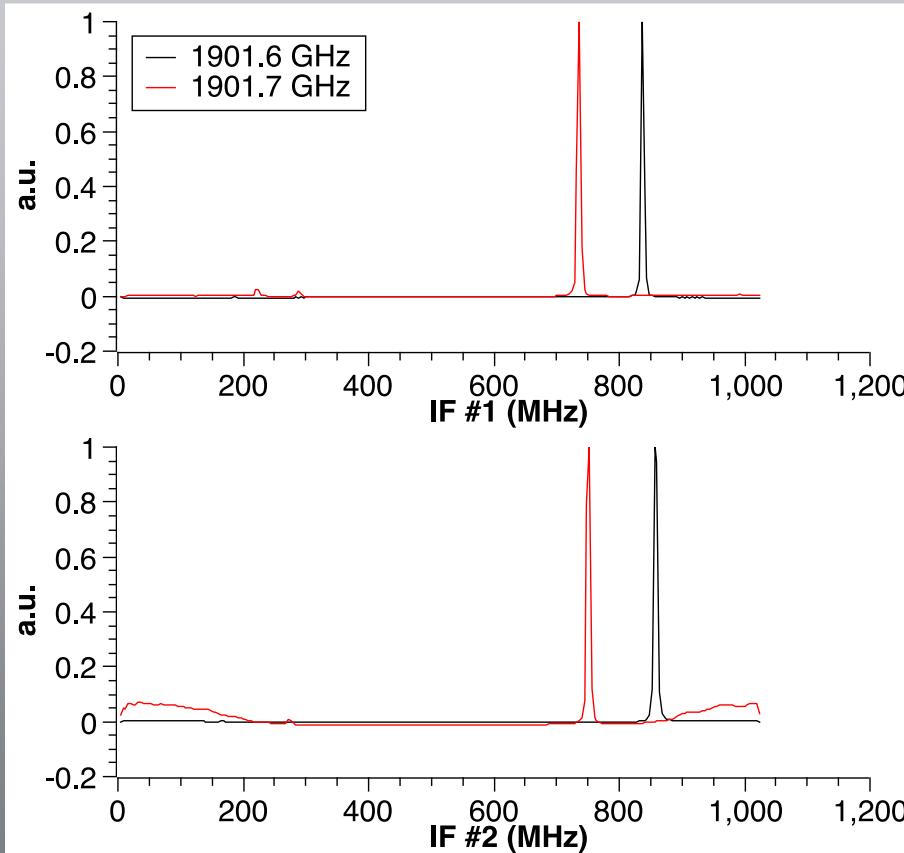
## 2.0 GHz/s Specs

### 2.0 GS/s Complex FFT Version

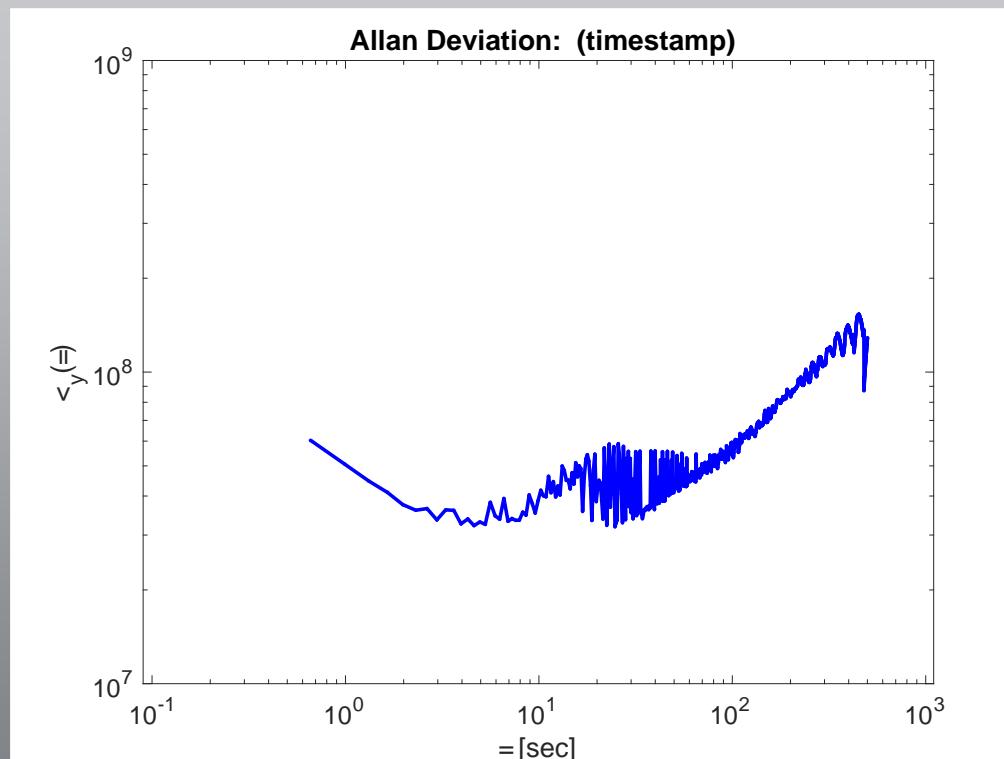
Parameter	Minimum	Typical	Maximum	Unit
Power Consumption	-	500	700	mW
Dynamic Range	-28	0	+5	dBm
Clock Frequency	1	-	2000	MHz
Bandwidth	-	6000	8000	MHz
Number of FFT channels (IQ)	-	512	-	MHz
Number of FFT channels (DSB)	-	256	-	Channels



# CMOS Spectrometer Processor Testing



# End-to-End Receiver Stability



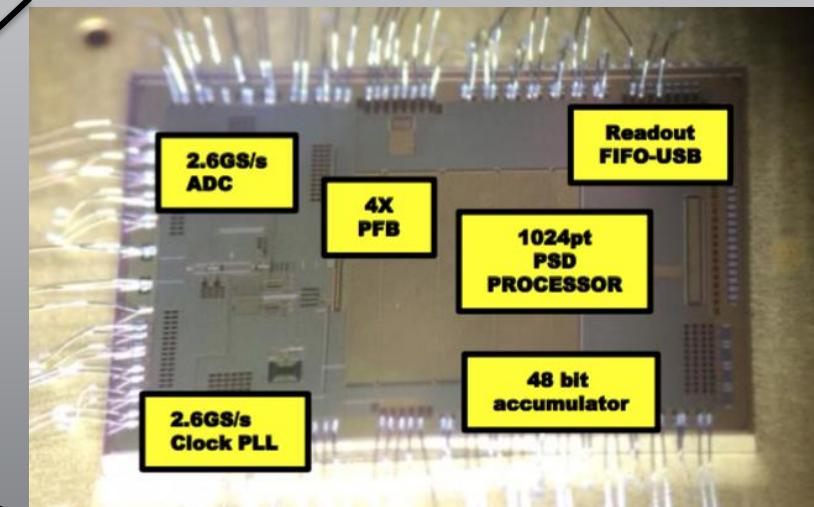
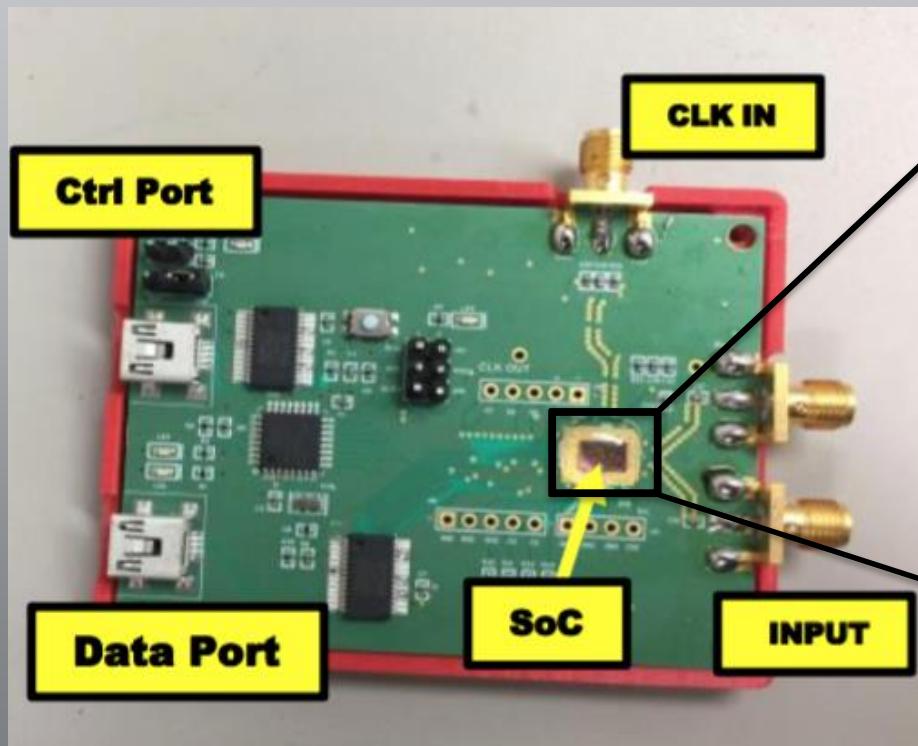
Spectrometer stability  
was longer than 1000 s.

End-to-end stabilized  
spectroscopic Allan  
Variance  $\sim 10$  s

Stabilized output LO  
power at 1.9 THz through  
a PID loop between the  
HEB mixer current and  
LO 660 GHz doubler bias  
voltage.

# CMOS Spectrometer Processor Development

**2.6 GS/s Real FFT Version**





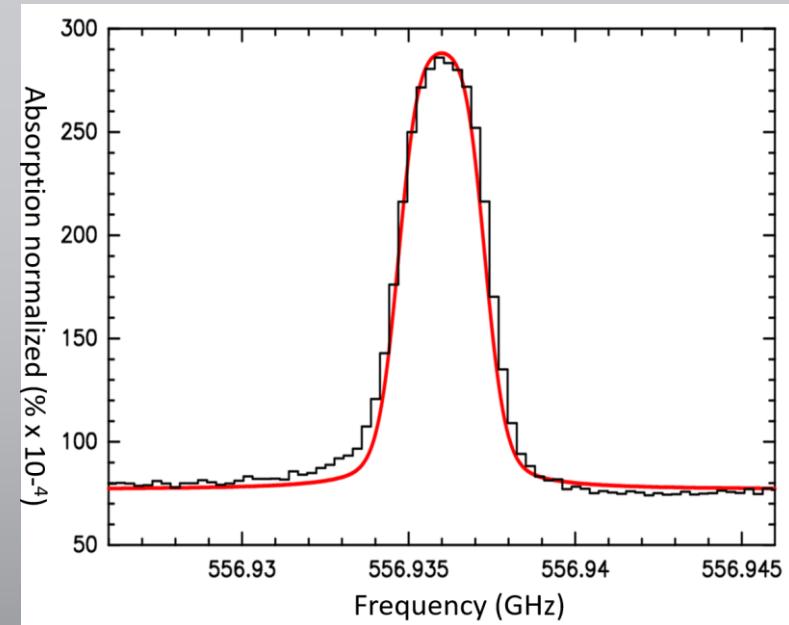
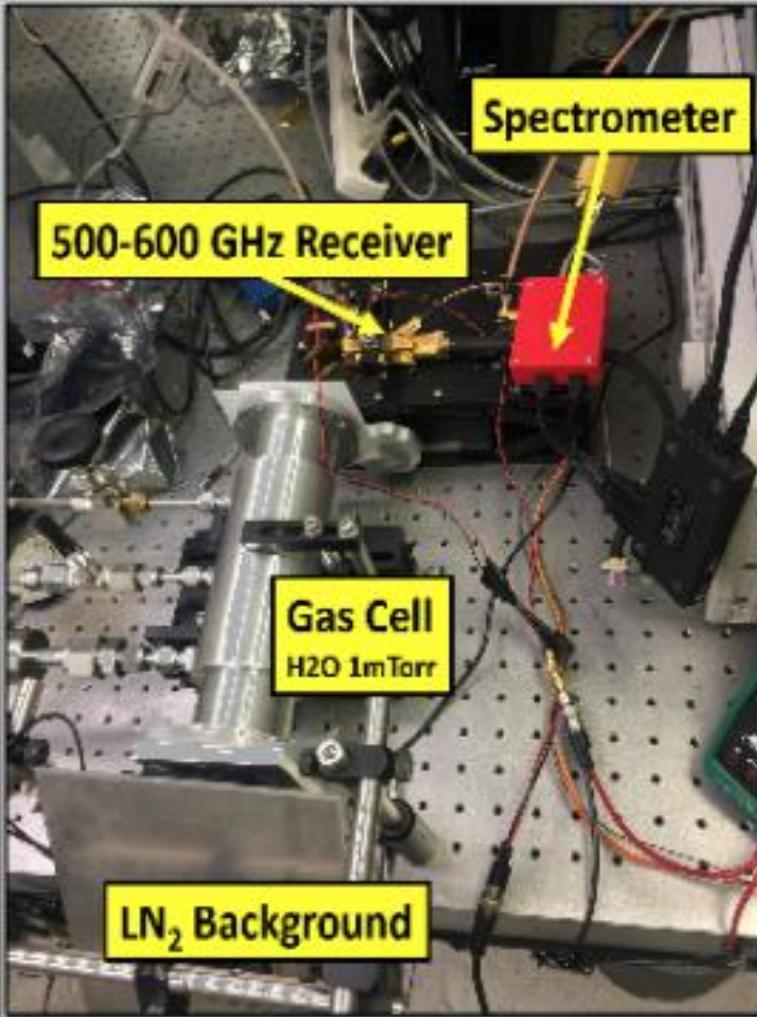
# CMOS Spectrometer

## 2.6 GHz/s Specs

### 2.6 GS/s Real FFT Version

Parameter	Minimum	Typical	Maximum	Unit
Power Consumption	-	500	700	mW
Dynamic Range	-5	0	+5	dBm
Clock Frequency (PFB enabled)	1	-	2000	MHz
Clock Frequency (PFB disabled)	1	2000	2600	MHz
Bandwidth	-	-	9000	MHz
Number of FFT channels	-	1024	-	Channels

# CMOS Spectrometer Processor Testing

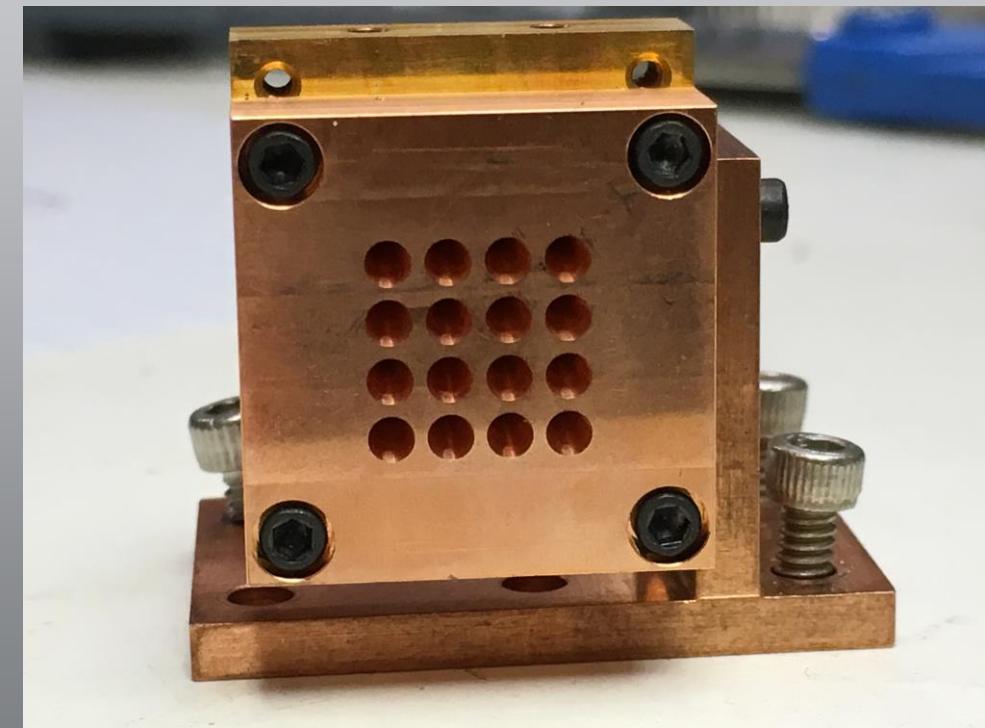
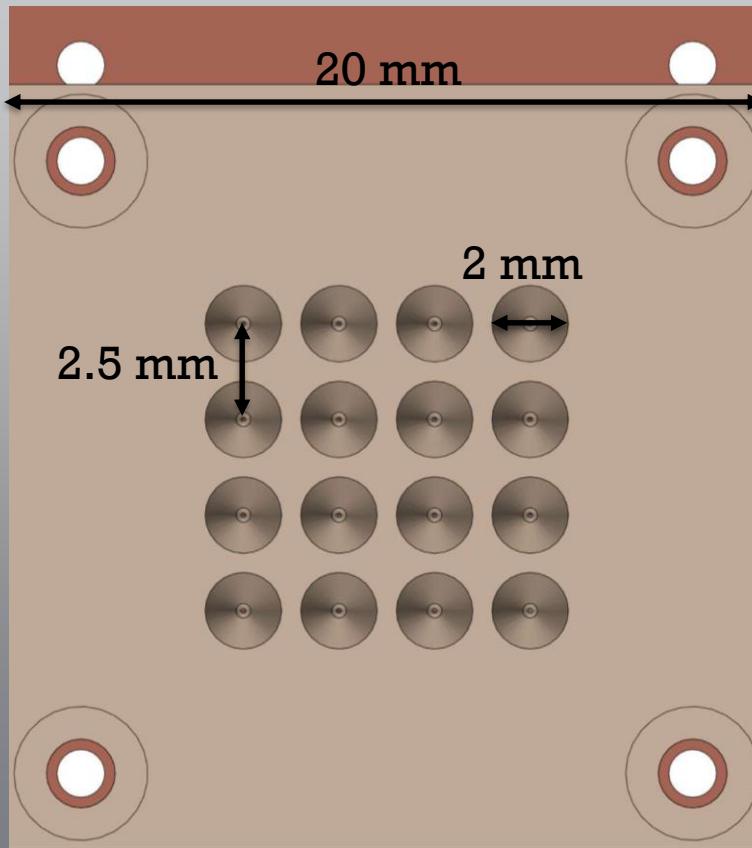


**Measured by  
Spectrometer Chip**

**Expected from H<sub>2</sub>O  
abundance and  
temperature**

# 16-Pixel Mixer Prototype Block

Next steps ...





# Summary

We have demonstrated a compact end-to-end test of a 4x1-pixel heterodyne array receiver at 1.9 THz.

- High sensitivity ~900 K DSB for best pixels
- Stability with CMOS spectrometer ~10 s
- The design is scalable in both frequency and number of pixels
- 16-pixel array has been designed and is currently under test

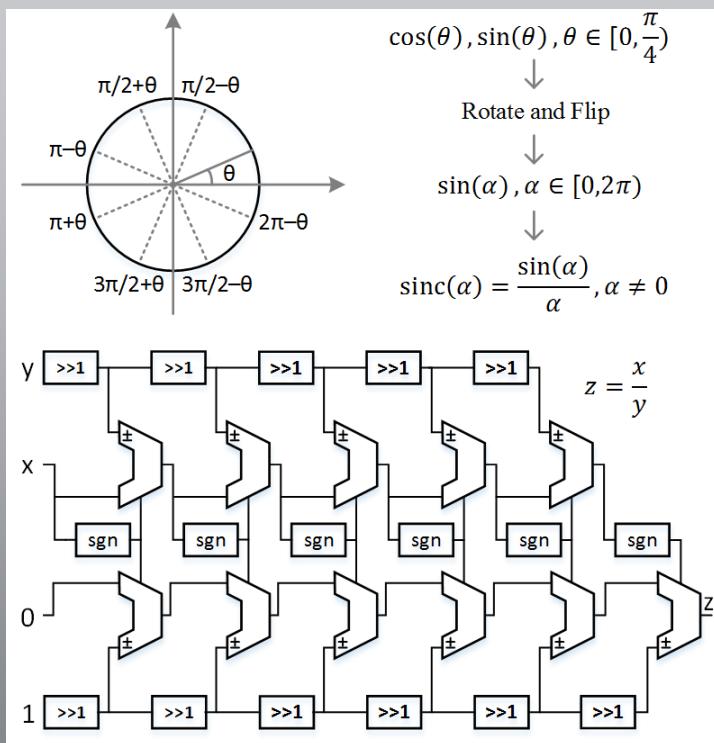
CMOS technology creates a compact spectrometer with low power consumption.



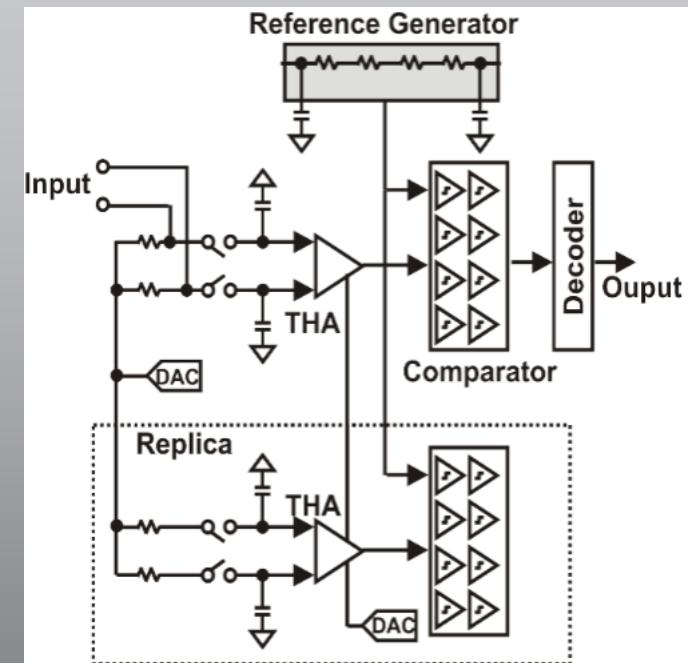
# **BACK UP SLIDES**

# CMOS Spectrometer Processor Development

## Poly-Phase Window Generation



## 3B /3GS Flash ADC



Integrated PLL for clock generation, radiation sensors, and calibration circuitry for tuning clock skew on each digital block and bias tuning all the ADC sub-circuits.

# CMOS Spectrometer Processor Development

## Interleaved FFT Processor Core

